# UDAY MALLAPPA

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## RESEARCH INTERESTS

Design of efficient machine learning accelerators and network-on-chip routing algorithms. Reinforcement learning and Graph convolution based predictive models for complex physical design optimization tasks and network-on-chip routing.

## SKILLS

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|---|---|
| **Languages** | Python, CUDA, Perl, Tcl, C++, System Verilog |
| **EDA Tools** | Quartus, Design Compiler, PrimeTime, Tempus, IC Compiler Innovus, RedHawk and HSPICE |
| **Math/Statistics Tools** | Matlab, CPLEX, Z3 SMT/SAT Solver |

## EDUCATION

Ph.D. in Electrical and Computer Engineering — Sep. 2017 - Present
**University of California** — San Diego
Advisors: Prof. C. K. Cheng and Prof. Tajana Rosing — (CGPA: 3.9/4.00)
Related Courses: VLSI Digital System Algorithms and Architectures, VLSI Integrated Circuits and Systems Design, Algorithmic & Optimization Foundations for VLSI CAD, Principles of Computer Architecture, Advanced Microarchitecture (Accelerated Learning), Principles of AI: Probabilistic Reasoning & Decision-Making, AI: Learning Algorithms, Design & Analysis of Algorithms, AI: Search & Reasoning, Numerical Optimization Methods, Introduction to Operating Systems, and GPU Programming (for parallel data processing).

B.E. & M.S (Dual Degree in Electrical & Electronics Engineering, Physics) — Aug. 2006 - Jul. 2011
**BITS-Pilani** — India

## WORK EXPERIENCE

**SEE Lab, University of California - San Diego** — Jan. 2021 - Present

- Combine hyperdimensional computing and convolution neural networks to mitigate the compute and memory bottlenecks of image classification tasks.
- Architecural and algorithmic innovation to design an efficient (in terms of power, performance and area) CNN accelerator ($40nm$ technology). The goal of this project is to tapeout an ASIC accelerator with an online-training functionality.

**NVIDIA Corp.** — Jun. 2020 - Dec. 2020
*Research & Development Intern (Reinforcement Learning)* — *Santa Clara, CA*

- Using reinforcement learning algorithms (control) for the placement-optimization problem.
- SAT-based optimization for the standard-cell detailed placement problem.

**VLSI Lab, Univesity of California at San Diego** — Sep. 2019 - Present

- Use graph convolutional networks for post-layout leakage-recovery prediction

– Use Satisfiability Modulo Theories (SMT) for application-specific deadlock-free routing and VC assignment; combines routing and VC assignment into a single optimization problem to demonstrate improved latency curves (as compared to existing oblibious routing algorithms). This work involves in modification of existing cycle-accurate simulators for injection of custom traffic, enforcing custom routing and static VC assignment.

**Synopsys Inc.** Jun. 2019 - Sep. 2019
*Research & Development Intern (Machine Learning)* *Mountain View, CA*

– Using learning algorithms to predict downstream design outcomes. In particular, the goal is to predict crosstalk delay at pre-route stage of the design, that eventually guides routing optimization engine and improves design convergence.

**VLSI CAD Lab, University of California at San Diego** Sep. 2017 - June 2019
*Graduate Student Researcher* *La Jolla, CA*

– Machine learning in EDA to accelerate design convergence. In particular, using machine learning models to reduce heavy runtimes invested in timing analysis, without loss of accuracy.
– Integer Linear Programming and Simulated Annealing for memory placement of IC design.
– CNN-based Power Delivery Network synthesis for improved signal routability.

**Intel Corp** Jan.2016 - Aug 2017
*SOC Design Engineer* *Bangalore, India*

– RTL-GDS physical implementation and SoC power optimization for $10nm$ baseband processors.

**Qualcomm, Inc** Nov. 2012 - Jan. 2016
*Senior Engineer* *Bangalore, India*

– SoC Power Delivery Network Signoff for sub-$28nm$ technology nodes.
– SoC Chip-Package co-analysis, thermal, ESD analysis for sub-28nm technology nodes.

**ANSYS, Inc** Aug. 2011 - Nov. 2012
*Engineer* *Bangalore, India*

– Clock-Jitter analysis using Apache Timing Engine.

**Hewlett-Packard - Imaging and Printing R & D Hub.** Jan. 2011 - Jul. 2011
*Research Intern* *Bangalore, India*

– Image processing algorithms for shadow removal applications, intended for HP 3-D scanners.

## PUBLICATIONS

All papers with Prof. Andrew B. Kahng, have authors listed in alphabetical order by last name.


[1] A. B. Kahng, **U. Mallappa**, L. Saul, "Using Machine Learning to Predict Path-Based Slack from Graph-Based Timing Analysis", *Proc. ICCD*, 2018.

[2] A. B. Kahng, **U. Mallappa**, L. Saul and S. Tong, "Unobserved Corner Prediction: Reducing Timing Analysis Effort for Faster Design Convergence in Advanced-Node Design", *Proc. DATE*, 2019. (**nominated for Best Paper award**)

[3] T. Ajayi, V. A. Chhabria, M. Fogaca, S. Hashemi, A. Hosny, A. B. Kahng, M. Kim, J. Lee, **U. Mallappa**, M. Neseem, G. Pradipta, S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, M. Shalan, W. Swartz, L. Wang, Z. Wang, M. Woo and B. Xu, "Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project", *Proc. DAC* 2019.

[4] V. Chabbria, A. B. Kahng, M. Kim, **U. Mallappa**, S. Sapatnekar and B. Xu "Template-based PDN Synthesis in Floorplan and Placement Using Classifier and CNN Techniques", *Proc. ASPDAC*, 2020.

[5] U. Mallappa and C. K. Cheng, "GRA-LPO: Graph Convolution Based Leakage PowerOptimization", *Proc. ASPDAC*, 2021.

[6] U. Mallappa, S. Pratty and D. Brown, "RLPlace: Deep RL Guided Heuristics for Detailed Placement Optimization", *Proc. DATE*, 2022.

[7] U. Mallappa, C. K. Cheng and B. Lin, "Joint Application-aware oblivious-Routing and Static VC Allocation (JARVA)", *Embedded Systems Letters*, 2022.

[8] U. Mallappa et al., "PatterNet: Explore and Exploit Filter Patterns for Efficient Deep Neural Networks", *Proc. DAC*, 2022.

## OTHER ACTIVITIES

UCSD ECE department fellowship, Sep. 2017 - June 2018.

Teaching assistant for ECE 260A/B, CSE 140 and CSE 140L. Recognized by UCSD CSE, for exceptional contributions.

General secretary of physics society, Panel-coordinator for annual technical festival, BITS-Pilani